

Amendment and Response

Applicant: Trudy L. Benjamin
Serial No.: 10/827,142
Filed: April 19, 2004
Docket No.: 200309559-1
Title: FLUID EJECTION DEVICE

REMARKS

The following Remarks are made in response to the Non-Final Office Action mailed March 17, 2006 in which claims 1-64 were rejected. With this amendment, claim 64 has been cancelled without prejudice and claims 1, 3-9, 12, 13, 22-27, 29-34, 40-42, 44-56, 58-61, and 63 have been amended. Claims 1-63 remain pending in the application and are presented for reconsideration and allowance.

Claim Objections

Claims 12 and 13 are objected to because of the following informalities: both claims repeat the word "substantially."

Claims 12 and 13 have been amended to remove one of the repeated words in each of the two claims. Applicant respectfully requests that the claim objections be removed.

Claim Rejections under 35 U.S.C. § 102 and § 103

Claims 1-12, 22-26, 29, 30, 33-41, 43, 48, 49, 51, 52, 54, 63, and 64 are rejected under 35 U.S.C. § 102(b) as being anticipated by the Hayasaki European Patent No. 1128324.

Claims 58-60 are rejected under 35 U.S.C. § 103(a) as being unpatentable over the Hayasaki European Patent No. 1128324 in view of the Feinn et al. US Patent Application No. 2003/0071028.

Claims 13-15, 42, 44-47, 50, 53, and 55-57 are rejected under 35 U.S.C. § 103(a) as being unpatentable over the Hayasaki European Patent No. 1128324 in view of the Axtell et al. US Patent Application No. 2002/0093551.

Claims 16-21 are rejected under 35 U.S.C. § 103(a) as being unpatentable over the Hayasaki European Patent No. 1128324 and the Axtell et al. US Patent Application No. 2002/0093551, and further in view of the Tabata et al. Japan Patent No. 6-79873.

Claims 27, 28, 31, and 32 are rejected under 35 U.S.C. § 103(a) as being unpatentable over the Hayasaki European Patent No. 1128324 in view of the Tabata et al. Japan Patent No. 6-79873.

Claims 61 and 62 are rejected under 35 U.S.C. § 103(a) as being unpatentable over the Hayasaki European Patent No. 1128324 and the Feinn et al. US Patent Application No. 2003/0071028, and further in view of the Tabata et al. Japan Patent No. 6-79873.

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The Hayasaki Patent is directed to a printhead, which receives an image data signal that includes a 4-bit bus format containing block selection data in its head. The image data signal is separated by a selection signal and only the block selection data contained in the head is held in a latch and supplied to a decoder. The 4-bit image data corresponding to four segments is held in four latches of a first printing control unit. The printhead includes a plurality of printing elements and the block selection circuit for outputting a selection signal to select a block of the plurality of printing elements that can be simultaneously driven. The printhead also includes the printing control circuit for outputting a driving signal for selectively driving the printing elements, together with the selection signal and in correspondence with the image data.

Amended independent claims 1, 9, 23, 40, 48, 51, and 58 and independent claim 35 include limitations related to providing a sequence of address signals. Applicant submits that the Hayasaki Patent fails to teach or suggest providing a sequence of address signals. In contrast, in the Hayasaki Patent, an image data signal includes block selection data in its head and image data. The block selection data contained in the head is held in a latch and supplied to a decoder. This block selection circuit outputs a selection signal to select one block of the plurality of printing elements that can be simultaneously driven. The selection signal selects one block at a time and not a sequence of blocks.

Amended independent claims 1, 9, 23, 40, 48, 51, and 58 and independent claims 35 also include limitations related to providing a first sequence of address signals and a second sequence of address signals. The Hayasaki Patent fails to teach or suggest providing a first sequence of address signals and a second sequence of address signals. In contrast, in the Hayasaki Patent, image data and block selection data are continuously transferred over the data bus and internally separated and used. Only the block selection data contained in the head is held in a latch and supplied to a decoder, which outputs a selection signal to select one block of the plurality of printing elements that can be simultaneously driven. The 4-bit image data corresponding to four segments is held in four latches of a first printing control unit. Neither the selection signal that selects one block of the plurality of printing elements nor the image data is a sequence of address signals.

Amended independent claims 1, 40, and 48 and independent claim 35 also include limitations related to initiating or selectively initiating the first sequence of address signals

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and the second sequence of address signals in response to a control signal. The Hayasaki Patent fails to teach or suggest initiating or selectively initiating a first sequence of address signals and a second sequence of address signals in response to a control signal. In contrast, in the Hayasaki Patent, the printhead receives control signals, such as the image data signals, a clock signal, a latch signal for defining a driving period, and driving signals. The image data signals include image data and block selection data, which are internally separated and used. The clock signal clocks in the image data signal and the latch signal latches in the image data and block selection data. None of these control signals are used to initiate or selectively initiate a first sequence of address signals and a second sequence of address signals.

Amended independent claims 1 and 48 also include limitations related to a first pulse of the control signal that initiates the first sequence of address signals and a second pulse of the control signal that initiates the second sequence of address signals. The Hayasaki Patent fails to teach or suggest a first pulse of a control signal initiating a first sequence of address signals and a second pulse of the control signal initiating a second sequence of address signals. In contrast, in the Hayasaki Patent, the printhead receives control signals, such as the image data signals, a clock signal, a latch signal for defining a driving period, and driving signals. The clock signal clocks in the image data signal and the latch signal latches in the image data and block selection data. None of these control signals include a first pulse to initiate or selectively initiate a first sequence of address signals and a second pulse to initiate or selectively initiate a second sequence of address signals.

Amended independent claims 9, 23, and 58 and independent claim 35 include limitations related to an address generator or first address control circuit that provides or generates or selectively initiates a first sequence of address signals and a second sequence of address signals. The Hayasaki Patent fails to teach or suggest an address generator or first address control circuit that provides or generates or selectively initiates a first sequence of address signals and a second sequence of address signals. In contrast, in the Hayasaki Patent, image data and block selection data are continuously transferred over the 4-bit data bus and internally separated and used. Only the block selection data contained in the head is held in a latch and supplied to a decoder, which outputs the selection signal to select one block of the plurality of printing elements that can be simultaneously driven. The 4-bit image data is held

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in four latches of a first printing control unit. Neither the selection signal that selects one block of the plurality of printing elements nor the image data is a sequence of address signals.

Amended independent claims 9 and 51 include limitations related to the second sequence of address signals being selectively provided independent of the first sequence of address signals. The Hayasaki Patent fails to teach or suggest a second sequence of address signals being selectively provided independent of a first sequence of address signals. In contrast, in the Hayasaki Patent, block selection data contained in the head is held in a latch and supplied to a decoder, which outputs a selection signal to select one block of the plurality of printing elements that can be simultaneously driven. The selection signal is not a sequence of address signals and a second sequence of address signals is not provided independently of a first sequence of address signals via the block selection circuit in one or more address generators.

Amended independent claims 23 and 58 include limitations related to an address generator that includes first bank circuitry configured to receive a first group of timing pulses and generate a first sequence of address signals in response to the first group of timing pulses and second bank circuitry configured to receive a second group of timing pulses and generate a second sequence of address signals in response to the second group of timing pulses. The Hayasaki Patent fails to teach or suggest these limitations. In contrast, in the Hayasaki Patent, each block selection circuit receives the clock signal and the latch signal. The clock signal clocks in the image data signal and the latch signal latches in the image data and block selection data. Also, each block selection circuit receives the block selection data contained in the head of the image data signal and outputs a selection signal to select one block of a plurality of printing elements that can be simultaneously driven. None of these control signals include a first group of timing pulses for generating a first sequence of address signals and a second group of timing pulses for generating a second sequence of address signals.

In view of the above, Applicant submits that all features of amended independent claim 1, all features of amended independent claim 9, all features of amended independent claim 23, all features of independent claim 35, all features of amended independent claim 40, all features of amended independent claim 48, and all features of amended independent claim 51 are not taught or suggested by the Hayasaki Patent.

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The Examiner further relies on the Feinn et al. publication as a basis for the § 103 obviousness rejection of independent claim 58. Applicant respectfully submits that the Feinn et al. publication does not teach or suggest the above limitations of amended independent claim 58.

In view of the above, Applicant submits that all features of amended independent claim 58 are not taught or suggested by the Hayasaki Patent and the Feinn et al. publication alone or in combination.

Dependent claims 3-8, 12, 13, 22, 24-27, 29-34, 41-42, 44-47, 49-50, 52-56, and 59-61 have been amended to clarify the claims. Also, dependent claim 63 has been amended to depend from amended independent claim 58 and dependent claim 64 has been cancelled without prejudice. Dependent claims 2-8 further define patentably distinct amended independent claim 1. Dependent claims 10-22 further define patentably distinct amended independent claim 9. Dependent claims 24-34 further define patentably distinct amended independent claim 23. Dependent claims 36-39 further define patentably distinct independent claim 35. Dependent claims 41-47 further define patentably distinct amended independent claim 40. Dependent claims 49-50 further define patentably distinct amended independent claim 48. Dependent claims 52-57 further define patentably distinct amended independent claim 51. Dependent claims 59-63 further define patentably distinct amended independent claim 58. Accordingly, dependent claims 2-8, 10-22, 24-34, 36-39, 41-47, 49-50, 52-57, and 59-63 are also believed to be allowable.

Therefore, Applicant respectfully requests that the above rejections under 35 U.S.C. § 102 and § 103 be withdrawn and claims 1-63 be allowed.

CONCLUSION

In view of the above, Applicant respectfully submits that pending claims 1-63 are all in a condition for allowance and requests reconsideration of the application and allowance of all pending claims.

The Examiner is invited to contact the Applicant's representative at the below-listed telephone numbers to facilitate prosecution of this application.

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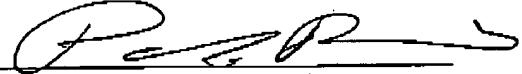
Respectfully submitted,

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CERTIFICATE UNDER 37 C.F.R. 1.8: The undersigned hereby certifies that this paper or papers, as described herein, are being facsimile transmitted to the United States Patent and Trademark Office, Fax No. (571) 273-8300 on this 17 day of July, 2006.


By _____
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